REMARKS

Status

This Amendment is in response to the Office Action mailed 10/05/2005 in which Claims 76, and 92-93 were objected to, Claims 76-93 were rejected under 35 USC 112, and Claims 76-93 were variously rejected under 35 USC 102 and 103.

Claims 76, 77, 78, 79, 81, 86, 87, 88, 91, 92, and 93 have been amended.

Claims 1-76, 82-83, and 94-104 have been cancelled.

Claims 76- 81, and Claims 84-93 remain in the application.

Claim Objection

Claims 76, 92, and 93 have been amended to obviate the language objections raised by the Examiner. As amended, Claims 76, 92, and 93 are deemed to satisfy the requirements of the Patent Statute and it is therefore requested that the objection to these claims be reconsidered and withdrawn.

Claim Rejections – 35 USC 112

Claims 76-93 have been rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims have been amended to obviate this rejection. The pending Claims 76-81 and 84-93 are deemed to satisfy all of the requirements of the Patent Statute and it is requested that the 112 rejection be reconsidered and withdrawn.

Claim Rejections – 35 USC 102 and 103

The rejection of Claims 76, 82-86, 91-92 under 35 USC 102(e)/(a) as being anticipated by Okabe, the rejection of Claims 79-91, 87, 88-90, 93 under 35 USC 103(a) as being unpatentable over Okabe, Iwai, and Yamane, the rejection of Claims 76, 79, 82-87, 91 under 35 USC 103(a) as being unpatentable over Kubo and Pruniaux, the rejection of Claims 92-93 under 35 USC 103(a) as being unpatentable over Kubo, Pruniaux, and Okabe, and the rejection of Claims 80-81, 88-90 under 35 USC 103(a) as being unpatentable over Kubo, Pruniaux, and Iwai are traversed.

According to the invention, there is provided a method for making a planar semiconductor device, comprising a semiconductor substrate having a first surface and second, opposite and planar surface and a lowered electrical resistivity. The method includes forming a highly doped drain region in the second, planar surface, and in the first surface, forming one or more device active regions above the drain region, the device active regions comprising one or more wells of dopants of a second and opposite polarity and in the wells one or more source regions of dopants of a first polarity, the sources laterally spaced from each other; and forming gate regions over portions of the well regions between the source regions and the drain region. The method also comprises in the second, planar surface of the substrate after forming the highly doped drain region, forming one or more recesses extending from the second, planar surface of the substrate into interior portions of the semiconductor substrate, wherein the one or more recesses occur between planar regions of the second surface, forming resistivity lowering bodies in the one or more recesses to fill the one or more recesses, the resistivity lowering bodies comprising a material different than the semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate, and forming a planar electrical contact layer over the second planar surface of the substrate and in electrical contact with the one or more resistivity lowering bodies.

The cited references clearly do not anticipate or make obvious the present invention, taken alone or in combination. Okabe has been cited as anticipating the invention. It is an established principle of patent law that for a reference to anticipate, the reference must disclose each and every element of the claimed invention. Okabe clearly fails this test. Okabe discloses grinding the surface of the bottom layer of the semiconductor substrate "to have a concavo-convex surface which has many course surface irregularities. Therefore, the ohmic electrode 26 can be firmly adhered to the ground surface 22 because the ground surface 22 has a suitable concavo-convex surface" (Okabe, Col. 4, lines 15-19). The concavo-convex surface is clearly not anticipatory of the recesses of the claimed invention which occur between planar regions of the second surface of the substrate. Okabe Fig. 1 clearly shows that the ground surface is jagged with no planar surfaces between recesses. Moreover, as pointed out, the surface grinding of Okabe is carried out, not to reduce the on resistivity

of the semiconductor device, but rather to establish adherence between the ohmic layer and the semiconductor substrate. The lowering of the resistivity of the device in Okabe is done through the use of arsenic instead of antimony as a dopant in the silicon substrate. "Moreover, the resistivity of the silicon substrate 1 is also diminished because of the higher concentration of As included in the silicon substrate 1 as an impurity. Consequently, the resistance R3 of the silicon substrate 1 is also reduced" (Okabe, Col. 4, Lines 10-14). The rejected claims are clearly novel and nonobvious over Okabe.

It is submitted that Okabe is improperly combined with Iwai and Yamane to render unpatentable the rejected claims. Iwai discloses forming open recesses in a major substrate of a semiconductor substrate in order to improve gettering efficiency. The gettering is accomplished at the bottom of the recesses to obtain this efficiency. Filling up the recesses of Iwai with resistivity lowering bodies would render the Iwai manufacturing method inoperable. Thus, Iwai teaches away from the claimed invention. Yamane discloses grinding a semiconductor wafer to form a reticulate grinding groove to facilitate adherence to an envelope. There is no disclosure in Yamane of any solution to the problem of lowering the on-resistance of semiconductor devices as in the claimed invention. The stated problems to be solved by the disclosures of both Yamane and Iwai are inapplicable to the problems solved by the present invention. It is submitted that the rejected claims are clearly patentable over these references.

The claimed invention has also been rejected as unpatentable over Kubo and Pruniaux. Kubo has the same deficiencies as Iwai in disclosing forming open grooves in the back surface of a semiconductor substrate. This is in contrast with the claimed invention wherein the recesses are filled with resistivity-lowering bodies. Puniaux discloses a mesa type field effect transistor having an electrode 16 which penetrates deeply into the semiconductor substrate. The present invention is a method for making a planar semiconductor device not a mesa device. The problems of making the two devices are quite different and solutions are not readily applicable from one technology to the other. Thus, the claimed method includes forming a planar electrical contact layer over the second planar surface of the substrate. Pruniaux discloses no planar electrical contact layer, but rather a massive electrode that penetrates deeply into

the semiconductor substrate. Clearly, neither reference taken alone or in combination renders unpatentable the rejected claimed invention.

Clearly the pending claims in the application are novel and nonobvious over the art of record and should be allowed.

Summary

The application as amended is patentable over the art of record as that art is applied to the claims and a notice of allowance is respectfully requested.

Respectfully submitted,

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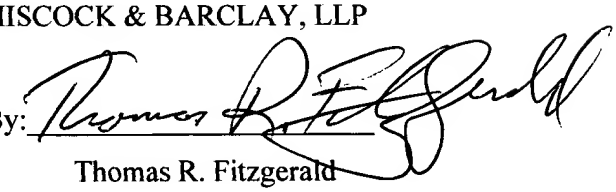
By: 

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